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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/631,921	07/31/2003	Jigish D. Trivedi	MICRON.104DV1	9664

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EXAMINER	
POMPEY, RON EVERETT	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/631,921	TRIVEDI, JIGISH D.	
	Examiner	Art Unit	
	Ron E. Pompey	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-12,14-18,20-26 and 28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-12,14-18,20-26 and 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 4-12, 14-18, 20-26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura (US 4,935,380) in further view of the admitted prior art (APA) and Yoo (US 5,605,854).

Okumura discloses the limitations of:

forming a gate stack on a substrate, the gate stack having at least one conductive layer, of tungsten silicide, (205, fig. 7B) and a source layer of polysilicon (213, fig. 7B) positioned on top of the at least one conductive layer and at an uppermost surface of the gate stack, the source layer providing a source of silicon (col. 6, ln. 59 – col. 7, ln. 9).

3. Okumura fails to disclose the limitations of:

exhuming a first layer of the gate stack so as to expose a portion of the source layer above at least a portion of the gate stack so as to define a first circuit node, comprises removing a portion of a cap insulating layer;

depositing a refractory material, of titanium so that the refractory material contacts the exposed uppermost portion of the source layer of the gate stack and so

that the refractory material is also positioned to contact a second circuit node of the integrated circuit having a rich source of the silicon;

forming a masking layer over the refractory material;

etching the masking layer so as to define an extent of the local interconnect;

selectively transforming the refractory material in a nitrogen containing ambient such that the refractory material underneath the etched masking layer including at the exposed portion of the source layer and the second circuit node is transformed into low resistance contacts wherein the source layer provides silicon to the portion of the refractory material positioned adjacent the exposed uppermost portion of the source layer and the second circuit node and wherein the refractory material beyond the extent of the local interconnect is transformed to comprise refractory material nitride; and

performing a selective removal process, such that the refractory material nitride and remaining refractory material beyond the extent of the local interconnect, with etchant (wet), is preferentially removed and wherein the contacts comprising refractory material silicide are preferentially unresponsive to the selective removal process;

wherein annealing the refractory material comprises exposing the refractory material to a rapid thermal processing environment having an N2/NH3 ambient so as to increase the temperature of the refractory material to a value between 600 degrees Celsius and 750 degrees Celsius for a period of time between 10 seconds and 60 seconds;

wherein the source layer provides the transforming atoms to the refractory material during transformation of the refractory material such that the selective removal

process reduces undercutting of the low resistance contact at the exposed surface of the source layer;

wherein the transforming of the refractory material comprises transforming the refractory material adjacent the source layer into a silicide contact and wherein the transforming atoms of the source layer comprise silicon atoms to transform the refractory material adjacent the source layer into the low resistance contact.

a. However, the admitted prior art (APA) discloses:

exhuming (202, fig. 1) a first layer (216, fig. 1) of the gate stack so as to expose uppermost surface of the gate stack so as to define a first circuit node;

depositing a refractory material, of titanium, (218, fig. 1) on the integrated circuit so that the refractory material contacts the exposed portion of the uppermost layer of the gate stack and so that the refractory material is positioned on second circuit node (206, fig. 1) of the integrated circuit having a rich source of transforming atoms; and

forming a masking layer (220, fig. 1) over the refractory material;

etching the masking layer so as to define an extent of the local interconnect;

selectively transforming the refractory material underneath the etched masking layer including at the exposed portion of the uppermost surface of the gate stack into a low resistance contact wherein the source layer provides silicon to the portion of the refractory material silicide positioned adjacent the exposed portion of the uppermost surface of the gate stack and the second circuit node;

performing a selective removal process, such that the refractory material nitride and remaining refractory material beyond the extent of the local interconnect, with

etchant (wet), is preferentially removed and wherein the contacts comprising refractory material silicide are preferentially unresponsive to the selective removal process (pg. 2, lns. 23-28);

wherein the source layer provides the silicon to the refractory material during transformation of the refractory material such that the selective removal process reduces undercutting of the low resistance contact at the exposed surface of the source layer;

wherein the transforming of the refractory material comprises transforming the refractory material adjacent the source layer into a silicide contact and wherein silicon is the source layer to transform the refractory material adjacent the source layer into the low resistance contact. (pg. 1, ln. 28 – pg. 3, ln. 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the admitted prior art with Okumura, because the uppermost layer of the gate stack, in Okumura (213, fig. 7B), protects the gate structure from subsequent process and the refractory material/silicide formed by the titanium, in APA, and the silicon uppermost layer of the gate stack, in Okumura, provides an electrical connection between circuit nodes in an integrated circuit.

b. However, Yoo discloses:

wherein annealing the refractory material comprises exposing the refractory material to a rapid thermal processing environment having an N2/NH3 ambient so as to increase the temperature of the refractory material to a value between 600 degrees Celsius and 750 degrees Celsius for a period of time between 10 seconds and 60

seconds; and wherein the refractory material is transformed to comprise refractory material nitride (col. 4, lns. 43-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Yoo with Okumura and the admitted prior art, because rapid thermal processing has less effect on the doping concentrations set in the previous process due to less prolonged heat treatment.

Response to Arguments

4. Applicant's arguments filed 2-27-06, pertaining to claims 1-2, 4-12, 14-18, 20-26 and 28, have been fully considered but they are not persuasive. The applicant argues that neither Okumura nor APA disclose ". . .selectively transforming the refractory material in a nitrogen containing ambient such that the refractory material underneath the etched masking layer and at least adjacent the exposed portion of the source layer and the second circuit node is transformed into low resistance contacts comprising refractory material silicide such that electrical contact between the refractory metal and the at least one conductive level occurs through the source layer and wherein the source layer provides silicon to the portion of the refractory material positioned adjacent the exposed uppermost portion of the source layer and wherein the refractory material beyond the extent of the local interconnect is transformed to comprise refractory material nitride; and

performing a selective removal process such that the refractory material nitride and remaining refractory material beyond the extent of the local interconnect is preferentially removed and wherein the contacts comprising refractory material silicide

are preferentially unresponsive to the selective removal process." (Claim 1 as currently amended). The applicant failed to argue why the Yoo reference does not address these issues of transforming the refractory material in a nitrogen containing ambient, which will further define the well-known high temperature annealing process used in the APA reference to transform the refractory material and following the further steps of the APA will provide the selective removal of the refractory material nitride and remaining refractory material beyond the extent of the local interconnect as described on page 2, line 23-28 in applicant's specification.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ron E. Pompey whose telephone number is (571) 272-1680. The examiner can normally be reached on compressed.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ron Pompey
AU: 2812
March 4, 2006

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER